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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,844	08/21/2003	Joseph A. Iadanza	BUR920030070US1	1843

30449 7590 11/18/2004

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,844	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,16-21 and 23* is/are rejected.

7)☒ Claim(s) *7,9-15,22 and 24-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a circuit [claim 1] must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. [See **Note** below]

2. The drawings are objected to because in Fig. 1 Clean GND 150 should be change to Clean GND 145. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. [See **Note** below]

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: ground node network 285 [see paragraph 0026]. [See **Note** below]

Note: Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 8, 16-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Koshikawa (5428299).

Regarding claims 1 and 16, Koshikawa et al discloses a voltage regulated power supply test circuit [see Fig. 5] comprising: a voltage regulator (built-in step down voltage generator 26) electrically connected to at least one regulated voltage node of a functional circuit (peripheral circuit 22) of an integrated circuit chip (semiconductor chip 21); and a circuit (monitoring circuit 25) capable of selectively connecting between one of said at least one regulated voltage nodes and ground with at least one load circuit (load transistors Qp16-17 and Qn18-19 or voltage divider 25b) adapted to put an emulated current load of said functional circuit (22) on said regulated voltage supply.

Regarding claims 2 and 17, Koshikawa et al discloses a reference voltage generator (reference voltage generator 23) electrically connected between said voltage regulator (26) and a power supply (Vext).

Regarding claims 3 and 18, Koshikawa et al discloses said power supply (Vext) is external to said integrated circuit chip (21) [see col. 5, lines 65-68].

Regarding claims 4 and 19, Koshikawa et al discloses said load circuit (voltage divider 25b) comprises a gated resistive load (R5 and R6).

Regarding claims 5 and 20, Koshikawa et al discloses said load circuit (load transistors Qp16-17 and Qn18-19) comprises a current mirror [see col. 7, lines 42-44].

Regarding claims 6 and 21, Koshikawa et al discloses means for varying the amount of current flowing through said load circuit.

Regarding claims 8 and 23, Koshikawa et al discloses at least one test point, each said at least one test point electrically connected to one of said at least one regulated voltage nodes.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kronlage (4227185), Iwata et al (5943282), Nair (6081105) and Ohlhoff (6504394) disclose a method and apparatus integrated circuit chip testing.

7. Claims 7, 9-15 and 22, 24-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 7 and 22, the primary reason for the allowance of the claims is due to the fact that the prior art does not disclose a current mirror that includes multiple mirror elements wherein each element is electrically connectable to different voltage sources having different on/off patterns.

Regarding claims 9 and 24, the primary reason for the allowance of the claims is due to the fact that the prior art does not disclose said one or more test points is an I/0 monitor pad of said integrated circuit chip.

Regarding claims 10 and 25, the primary reason for the allowance of the claims is due to the fact that the prior art does not disclose in combination multiple test points, each test point connected to a different regulated voltage node of said functional circuit, and a circuit capable of combining the voltages on each test point into a signal on one or more 1/0 monitor pads, a number of said monitor pads being less than a number of said test points. Since claims 11-13 depend from claim 10 and claims 26-28 depend from claim 25, they also have allowable subjected matter.

Regarding claims 14 and 29, the primary reason for the allowance of the claims is due to the fact that the prior art does not disclose said regulated voltage nodes are located on a regulated voltage grid. Since claim 15 depends from claim 15 and claim 30 depends from claim 30, they also have allowable subjected matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (517) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
November 15, 2004